REMARKS

Claims 1-5, 7-18, 20-22, 24-46, and 65 are pending in this application. Claims 6, 19, 23, and 47-64 are canceled herein. Claims 1, 7-11, and 20- 22 have been amended, and new claim 65 has been added herein. In view of these amendments and remarks, Applicant respectfully requests reconsideration of the claims.

Claims 33-46 have been allowed by the Examiner, and will not be discussed further.

Claims 1-32 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hara, *et al.* in view of Yasuda, *et al.* The applicant respectfully disagrees. More specifically, in his discussion of independent claim 1, the Examiner agrees that Hara, *et al.* does not disclose the elements of claim 1. However, the Examiner is of the opinion that "Figures 1-23 and the related text of the Yasuda, *et al.* reference discloses a first scribe line having a selected width extending along a first direction and adjacent a first die of the multiplicity of dies; a second scribe line having a selected width extending along a second direction adjacent the first die and intersecting the first scribe line at a corner point of the first die (Figures 3 and 6 of Yasuda, *et al.*); at least one free area defined on at least one of the first and second scribe lines where placement of a test key is restricted (Figures 14B) to provide an alignment method of aligning each of the processing areas on the wafer with a predetermined position at high speed and with accuracy even though the processing areas on the wafer are expanded, contracted, or rotated (Col. 4, lines 57-62). The Examiner then concludes it would have been obvious to form the scribe line of Yasuda, *et al.* in the invention of Hara, *et al.*

However, neither Figure 3 nor Figure 6 of Yasuda, *et al.* shows scribe lines. As is clear from column 5, line 13 and column 14, line 8 of the Yasuda, *et al.* specification, Figure 3 is a

diagram of an alignment mark image formed on the middle portion of index plate 22 of Figure 2. However as is clear from Figure 2, index plate 22 is part of the optical projection system and the alignment mark image of Figure 3 is not illustrated as being on a scribe line that separates adjacent semiconductor chips. Likewise, Figures 6A-6C are simply diagrams illustrating examples of two-dimensional alignment marks. As is well known by those skilled in the art, scribe lines basically represent the area between adjacent chips on a semiconductor wafer that is typically removed by a saw kerf (or other means) during separation or singulation of the multiplicity of chips on the wafer. There is simply no relationship between the alignment marks of Yasuda, *et al.* and scribe lines of the present invention. Figure 14B does show four "cross shaped" alignment marks at the four corners of chip 27-n, which marks are in the intersecting scribe lines. However, alignment marks are nothing like test keys, and independent claim 1 has been amended such that it now includes limitations no where even suggested much less taught by either the Hara, *et al.* or Yasuda, *et al.* references.

For example, independent claim 1 defines two restricted areas A_1 and A_S. Claim 1 also requires at least one test key to be located on the scribe lines but outside the restricted areas, and a second test key that is located in at least one of the two restricted areas, but only if the area of the test key is within certain defined parameters. Certainly neither Hara, *et al.* or Yasuda, *et al.* even mention the use of test keys on the scribe lines of a semiconductor wafer. They certainly do not teach of where a wafer may be located on a scribe line, and under what conditions the test keys can be located in certain restricted areas of the scribe line. Therefore, it is respectfully submitted that independent claim 1 is clearly now allowable over both Hara, *et al.* and Yasuda, *et al.* whether considered singly or in combination.

Consequently, it is further submitted that all claims that depend from claim 1 are also allowable for depending from a claim deemed allowable was well as for their own limitations.

In view of the above, Applicant respectfully submits that the application is in condition for allowance and requests that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicant requests that the Examiner contact Applicant's attorney at 972-732-1001 so that such issues may be resolved as expeditiously as possible. No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge the appropriate fees to Deposit Account No. 50-1065.

Respectfully submitted,

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Date

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